

IN THE CLAIMS:

1. (currently amended) A data processor, comprising:
a central processing unit; and
an address translation unit that receives a virtual addresses output from ~~said~~ the central processing unit and outputs a physical ~~address~~, addresses;
wherein ~~said~~ the address translation unit includes a first translation lookaside buffer, a second translation lookaside buffer, and a control circuit for selecting one of ~~said~~ the first and second translation lookaside buffers, wherein the address translation unit performs and performing address translation in accordance with an area of ~~an~~ a virtual address space ~~in said~~ of a virtual address received from the central processing unit.
2. (currently amended) A data processor according to claim 1,
wherein each of ~~said~~ the first and second translation lookaside buffers has a plurality of entries for holding ~~predetermined~~ physical addresses associated with a respective ~~predetermined~~ virtual ~~address-respectively~~ addresses for performing the address translation,
wherein ~~said~~ the central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space,
wherein ~~said~~ the first translation lookaside buffer translates ~~said~~ a virtual address of ~~said~~ the first virtual address space to ~~said~~ a physical address, and
wherein ~~said~~ the second translation lookaside buffer translates ~~said~~ a virtual address of ~~said~~ the second virtual address space to ~~said~~ a physical address.
3. (currently amended) A data processor according to claim 2,
wherein ~~a first entries of the part of entry means of said~~ plurality of entries in ~~said~~ the second translation lookaside buffer are controlled to be disabled from rewriting is, even when ~~said if the~~ second translation lookaside buffer detects an address translation miss, ~~disabled from rewriting the physical address stored in the entry~~, and
wherein ~~the remaining~~ second entries of ~~said~~ the plurality of entries in ~~said~~ the second translation lookaside buffer are controlled to be enabled for rewriting if the second translation lookaside buffer detects to rewrite the physical address stored in the entry at an address translation miss.
4. (currently amended) A data processor according to claim 3,

wherein ~~said part of entry means that is disabled from rewriting said physical address in said second translation lookaside buffer~~ the first entries store stores a physical address addresses for ~~storing~~ an address translation miss handling routine.

5. (currently amended) A data processor according to claim 4,
wherein it is determined whether or not ~~said~~ the plurality of entries in ~~said~~ the second translation lookaside buffer should be rewritten at an address translation miss in accordance with ~~said~~ the address translation miss handling routine.

6. (currently amended) A data processor according to claim 1,
wherein ~~said~~ the control circuit decodes upper bits of ~~the~~ a virtual address output from ~~said~~ the central processing unit and selects one of ~~said~~ the first and second translation lookaside buffers in accordance with a decode result.

7. (currently amended) A data processor according to claim 1,
wherein ~~said~~ the address translation unit further includes a selection circuit to which a first output of ~~said~~ the first translation lookaside buffer and a second output of the second translation lookaside buffer are input, ~~and which~~ wherein the selection circuit selects one of ~~said~~ the first and second outputs in accordance with ~~the~~ a control signal of ~~said~~ the control circuit ~~and outputs as said physical address.~~

8. (currently amended) A data processor according to claim 1,
wherein ~~said~~ the address translation unit further includes an address chop circuit that fixedly forms ~~said~~ a physical address from ~~said~~ a virtual address when both of ~~said~~ the first and second translation lookaside buffers are disabled.

9. (currently amended) A data processor according to claim 1,
wherein a page size of ~~said~~ the first translation lookaside buffer is different from a size of ~~said~~ the second translation lookaside buffer ~~at translation from the virtual address to the physical address.~~

10. (currently amended) A data processor according to claim 2,
wherein the number of ~~said~~ the plurality of entries included in ~~said~~ the first translation lookaside buffer is adapted so as to be larger than the number of ~~said~~ the plurality of entries included in ~~said~~ the second translation lookaside buffer, and

wherein a page size when ~~said~~ the first translation lookaside buffer translates ~~said~~ the virtual address of ~~said~~ the first virtual address space to ~~said~~ the physical address is adapted so as to be smaller than a page size when ~~said~~ the second translation lookaside buffer translates ~~said~~ the virtual address of ~~said~~ the second virtual address space to ~~said~~ the physical address.

11. (currently amended) A data processor according to claim 2,
wherein ~~said~~ the address translation unit further includes a third translation lookaside buffer having a plurality of entries for holding a predetermined physical ~~address~~ addresses associated with a predetermined virtual ~~address~~ addresses for performing address translation, and
wherein ~~said~~ the plurality of entries of ~~said~~ the third translation lookaside buffer is are capable of storing both ~~of~~ a copy of a part of the entries of ~~said~~ the plurality of entries in ~~said~~ the first address buffer and a copy of a part of the entries of ~~said~~ the plurality of entries in ~~said~~ the second address buffer.

12. (currently amended) A data processor according to claim 11,
wherein ~~said~~ the third address buffer is capable of operating selectively in accordance with an instruction fetch operation of ~~said~~ the central processing unit so as to perform address translation processing in parallel with ~~said~~ the first and second translation lookaside buffers.

13. (currently amended) A data processor, comprising:
a central processing unit; and
an address translation unit that receives virtual addresses output from ~~said~~ the central processing unit and outputs a physical ~~address~~; addresses;
wherein ~~said~~ the address translation unit includes a first translation lookaside buffer for performing address translation of a first virtual address space in ~~said~~ the virtual addresses, a second translation lookaside buffer for performing address translation of a second virtual address space in ~~said~~ the virtual addresses, and a control circuit for selecting ~~any~~ one of the ~~said~~ first and second translation lookaside buffers in accordance with whether a virtual address output from the central processing unit is in the first virtual address space or the second virtual address space ~~which of said~~ the ~~first and second virtual address spaces~~ ~~said virtual address belongs to and performing address translation.~~

14. (currently amended) A data processor according to claim ~~4~~ 13,

wherein each of ~~said the~~ first and second translation lookaside buffers includes a plurality of entries for holding a ~~predetermined~~ physical address, addresses respectively, associated with a ~~predetermined~~ virtual address addresses for performing address translation.

15. (currently amended) A data processor according to claim 1 ~~13~~,
wherein ~~said the~~ second translation lookaside buffer includes entries for ~~stores a physical address for storing~~ an address translation miss handling routine of ~~said the~~ first translation lookaside buffer, ~~and an entry for storing the physical address is~~ wherein the entries for the address translation miss handling routine are disabled from rewriting.

16. (currently amended) ~~An IP~~ A design data module including information of a microprocessor module, comprising:

data for defining an address translation unit for receiving a virtual address addresses output from a ~~predetermined~~ central processing unit and ~~outputs a~~ outputting physical address addresses,

wherein ~~said the~~ address translation unit includes a first translation lookaside buffer, a second translation lookaside buffer, and a control circuit for selecting one of ~~said the~~ first and second translation lookaside buffers, wherein the address translation unit performs ~~and for performing~~ address translation in accordance with an area of ~~an a~~ a virtual address space ~~in said of~~ a virtual address received from the central processing unit.

17. (currently amended) ~~An IP~~ A design data module according to claim 16,
wherein each of ~~said the~~ first and second translation lookaside buffers has a plurality of entries for holding ~~predetermined~~ physical addresses associated with a ~~predetermined~~ respective virtual address ~~respectively~~ addresses for performing the address translation,

wherein ~~said the~~ central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space,

wherein ~~said the~~ first translation lookaside buffer translates ~~said a~~ a virtual address of ~~said the~~ first virtual address space to ~~said a~~ a physical address, and

wherein ~~said the~~ second translation lookaside buffer translates ~~said a~~ a virtual address of ~~said the~~ second virtual address space to ~~said a~~ a physical address.

18. (currently amended) ~~An IP~~ A design data module according to claim 17,

wherein a first entries of the ~~part of entry means of said~~ plurality of entries in said the second translation lookaside buffer are controlled to be disabled from rewriting is, even when ~~said if the~~ second translation lookaside buffer detects an address translation miss, ~~disabled from~~ ~~rewriting the physical address stored in the entry,~~ and

wherein the remaining second entries of said the plurality of entries in the second translation lookaside buffer are controlled to be enabled for rewriting if the second translation lookaside buffer detects to rewrite the physical address stored in the entry at an address translation miss.